WHAT IS CLAIMED IS:

1. A memory circuit comprising:

a memory;

a delay circuit for generating a delay clock signal by delaying a reference clock signal;

at least one detection circuit for detecting a temperature of the memory or therearound, and/or a power-supply voltage of the memory or therearound; and

a control circuit for generating a control signal according to the temperature or the power-supply voltage detected by the detection circuit,

wherein a delay amount of the delay clock signal is controlled by the control signal.

2. A memory circuit according to Claim 1, further comprising a data capture circuit for capturing data read from the memory and/or data written into the memory, wherein the memory and/or the data capture circuit operates in synchronization with the delay clock signal.

3. A memory circuit according to Claim 1, wherein the delay circuit is formed as a PLL circuit or a DLL circuit.

4. A memory circuit according to Claim 2, wherein the delay circuit is formed as a PLL circuit or a DLL circuit.

5. A device including a memory circuit according to Claim 1, wherein image data output from the memory circuit is displayed.

6. A device including a memory circuit according to

Claim 2, wherein image data output from the memory circuit is displayed.

7. A device including a memory circuit according to Claim 3, wherein image data output from the memory circuit is displayed.

8. A device including a memory circuit according to Claim 4, wherein image data output from the memory circuit is displayed.

9. A device including a memory circuit according to Claim 1 and a plasma display panel, wherein image data output from the memory circuit is displayed by the plasma display panel.

10. A device including a memory circuit according to Claim 2 and a plasma display panel, wherein image data output from the memory circuit is displayed by the plasma display panel.

11. A device including a memory circuit according to Claim 3 and a plasma display panel, wherein image data output from the memory circuit is displayed by the plasma display panel.

12. A device including a memory circuit according to Claim 4 and a plasma display panel, wherein image data output from the memory circuit is displayed by the plasma display panel.

13. A method for operating a memory circuit including a memory, the method comprising the steps of:

generating a delay clock signal by delaying a reference clock signal;

detecting a temperature and/or a power-supply voltage of the memory; and

determining a delay amount of the delay clock signal according to the detected temperature and/or the detected power-supply voltage.

14. A method for operating a memory circuit including a memory, a first clock, and a second clock, the method comprising the steps of:

driving the memory in synchronization with the first clock;

capturing data read from the memory and/or data written into the memory in synchronization with the second clock;

detecting a temperature and/or a power-supply voltage of the memory or therearound; and

controlling a relative delay amount between the first clock and the second clock according to the detected temperature and/or the detected power-supply voltage.